R820T2 Register Description

Suite 808, Building 53, No.195, Sec.4, Chung Hsing Road, Chutung, HsinChu 310, Taiwan , R.O.C.
310 台灣新竹縣竹東鎮中興路四段 195 號 53 館 808 室
Tel: 886-3-5820868 Fax: 886-3-5820968 www.rafaelmicro.com

1 Programming and Registers

1.1 I2C Series Programming Interface

The programmable features of the R820T2 are accessible through an I2C compatible serial interface. Bi-directional data transfers are programmed through the serial clock (SCL) and serial data lines (SDA) at a standard clock rate of 100 KHz and up to 400KHz.

Data Transfer Logic

The I^2C control byte includes a fixed 7-bit slave address ID and a read/write (R/W) bit. Fixed I^2C slave address ID 0011010 (0x1A) is used for default setting. The R/W bit is set 0 for write and 1 for read (Table 1-1). Write mode and read mode will be further explained in the following sections.

I^2C Write/Read Address

Table 1-1 : I^2C Read / Write Address

I^2C Mode	I^2C Address(Bin)							R/W	Address (Hex)
	MSB							LSB	
Write Mode	0	0	1	1	0	1	0	0	0x34
Read Mode	0	0	1	1	0	1	0	1	0x35

Write Mode

When the slave address matches the I^2C device ID with write control bit , I^2C start interprets the following first byte as first written register address. These following bytes are all the register data (page write I^2C control). Register 0 to Register 4 are reserved for internal use only and can be written by I^2C write command.

Figure 1-1 : The Typical Write Mode Sequence

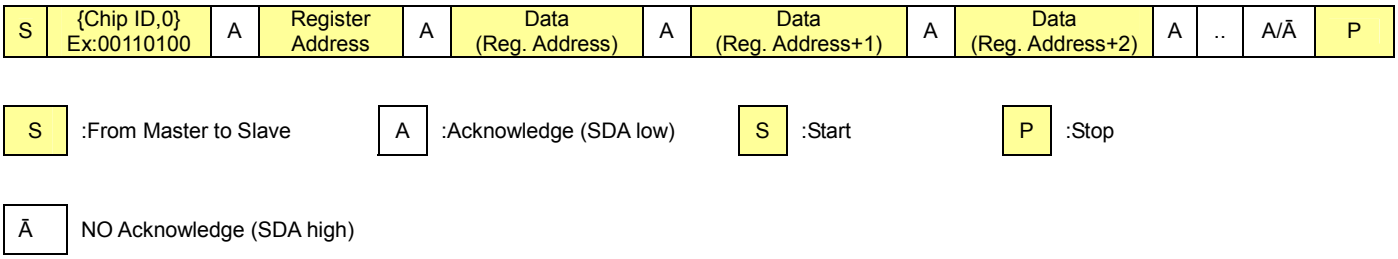
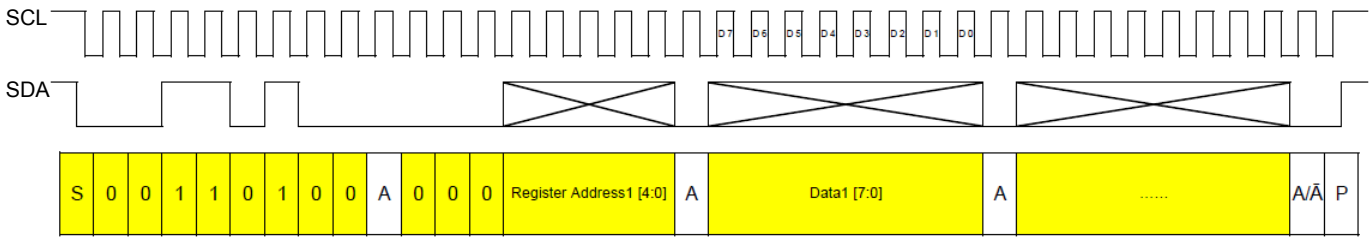


Figure 1-2 : An Example of Write Mode Procedure



Read Mode

When the slave address matches the I^2C device ID with read control bit, data are immediately transferred after ack command. Reading data transmission begins from core register 0 to final register until “P”(STOP) occurs. The data is transmitted from LSB to MSB, and the data of register 0 (0x96) is fixed as reference check point for read mode.

Figure 1-3 : The Typical Read Mode Sequence

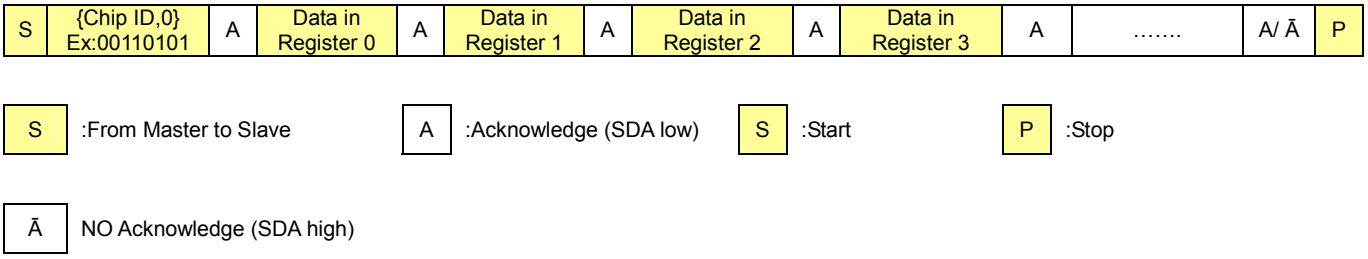
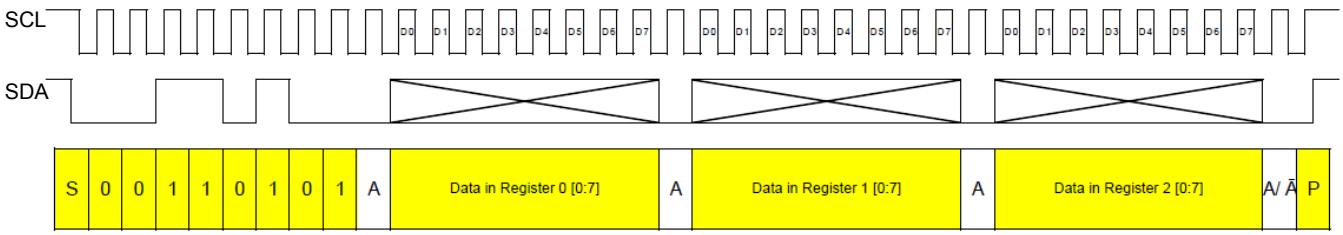


Figure 1-4 : An Example of Read Mode Procedure



1.2 Control Registers

Register Configuration

Total 32 registers are programmable to set the major functions of R820T2. The register matrix in table 1-2 outlines the structure of register bit. Detail register description is listed in the next section:

Table 1-2 : Register Matrix

Reg Address	Reg Name	Write /Read	B7	B6	B5	B4	B3	B2	B1	B0
0x00	R0	R	1	0	0	1	0	1	1	0
0x01	R1	R	-	-	-	-	-	-	-	-
0x02	R2	R	0	VCO_INDICATOR[6:0]						
0x03	R3	R	RF_INDICATOR [7:0]							
0x04	R4	R	-	-	-	-	-	-	-	-
0x05	R5	W/R	PWD_LT	0	PWD_LNA1	LNA_GAIN_MODE	LNA_GAIN[3:0]			
0x06	R6	W/R	PWD_PDET1	PWD_PDET3	FILT_3DB	1	0	PW_LNA[2:0]		
0x07	R7	W/R	0	PWD_MIX	PW0_MIX	MIXGAIN_MODE	MIX_GAIN[3:0]			
0x08	R8	W/R	PWD_AMP	PW0_AMP	IMR_G[5:0]					
0x09	R9	W/R	PWD_IFFILT	PW1_IFFILT	IMR_P[5:0]					
0x0A	R10	W/R	PWD_FILT	PW_FILT		1	FILT_CODE[3:0]			
0x0B	R11	W/R	0	FILT_BW[1:0]		0	HPF[3:0]			
0x0C	R12	W/R	1	PWD_VGA	1	VGA_MODE	VGA_CODE[3:0]			
0x0D	R13	W/R	LANVTH_H[3:0]				LNAVTH_L[3:0]			
0x0E	R14	W/R	MIXVTH_H[3:0]				MIXVTH_L[3:0]			
0x0F	R15	W/R	0	0	1	CLK_OUT_ENB	1	0	CLK_AGC_ENB	0
0x10	R16	W/R	SEL_DIV[2:0]			REF_DIV2	0	1	CAPX[1:0]	
0x11	R17	W/R	PW_LDO_A[1:0]		0	0	0	0	1	1
0x12	R18	W/R	1	0	0	0	PW_SDM	0	0	0
0x13	R19	W/R	0	0	0	0	0	0	0	0
0x14	R20	W/R	S_I2C[1:0]		N_I2C[4:0]					
0x15	R21	W/R	SDM_IN[8:1]							
0x16	R22	W/R	SDM_IN[16:9]							
0x17	R23	W/R	PW_LDO_D[1:0]		1	1	OPEN_D	1	0	0
0x18	R24	W/R	0	1	-	-	-	-	-	-
0x19	R25	W/R	PWD_RFFILT	0	0	SW_AGC	1	1	-	-
0x1A	R26	W/R	RFMUX[1:0]		1	0	PLL_AUTO_CLK[1:0]		RFFILT{1:0]	
0x1B	R27	W/R	TF_NCH[3:0]				TF_LP[3:0]			
0x1C	R28	W/R	PDET3_GAIN[3:0]				0	1	-	0
0x1D	R29	W/R	1	1	PDET1_GAIN[2:0]			PDET2_GAIN[2:0]		
0x1E	R30	W/R	0	1	PDET_CLK[4:0]					
0x1F	R31	W/R	1	1	0	0	0	0	-	-

1.3 Register Index and Description

Table 1-3 : R820T2 Register Index and Description

Reg	R/W	Bitmap	Symbol	Description
R5 0x05	R/W	[7]	PWD_LT	Loop through ON/OFF 0: on 1: off
	R/W	[5]	PWD_LNA1	LNA 1 power control 0:on 1:off
	R/W	[4]	LNA_GAIN_MODE	LNA gain mode switch 0: auto 1: manual
	R/W	[3:0]	LNA_GAIN[3:0]	LNA manual gain control 15: max gain : 0: min gain
R6 0x06	R/W	[7]	PWD_PDET1	Power detector 1 on/off 0: on 1: off
	R/W	[6]	PWD_PDET3	Power detector 3 on/off 0: off 1: on
	R/W	[5]	FILT_3DB	Filter gain 3db 0:0db 1:+3db
	R/W	[2:0]	PW_LNA[2:0]	LNA power control 000: max : 111: min
R7 0x07	R/W	[6]	PWD_MIX	Mixer power 0:off 1:on
	R/W	[5]	PW0_MIX	Mixer current control 0:max current 1:normal current
	R/W	[4]	MIXGAIN_MODE	Mixer gain mode 0:manual mode 1:auto mode
	R/W	[3:0]	MIX_GAIN[3:0]	Mixer manual gain control 0000->min 1111->max

Reg	R/W	Bitmap	Symbol	Description
R8 0x08	R/W	[7]	PWD_AMP	Mixer buffer power on/off 0: off 1:on
	R/W	[6]	PW0_AMP	Mixer buffer current setting 0: high current 1: low current
	R/W	[5:0]	IMR_G[5:0]	Image Gain Adjustment 0: min 63: max
R9 0x09	R/W	[7]	PWD_IFFILT	IF Filter power on/off 0: filter on 1: off
	R/W	[6]	PW1_IFFILT	IF Filter current 0: high current 1: low current
	R/W	[5:0]	IMR_P[5:0]	Image Phase Adjustment 0: min 63: max
R10 0x0A	R/W	[7]	PWD_FILT	Filter power on/off 0: channel filter off 1: on
	R/W	[6:5]	PW_FILT[1:0]	Filter power control 00: highest power 11: lowest power
	R/W	[3:0]	FILT_CODE[3:0]	Filter bandwidth manual fine tune 0000 Widest ……. 1111 narrowest

Reg	R/W	Bitmap	Symbol	Description
R11 0x0B	R/W	[6:5]	FILT_BW	Filter bandwidth manual course tunnel 00: widest 10 or 01: middle 11: narrowest
	R/W	[3:0]	HPF[3:0]	High pass filter corner control 0000: highest 1111: lowest
R12 0x0C	R/W	[6]	PWD_VGA	VGA power control 0: vga power off 1: vga power on
	R/W	[4]	VGA_MODE	VGA GAIN manual / pin selector 1: IF vga gain controlled by vagc pin 0: IF vga gain controlled by vga_code[5:0]
	R/W	[3:0]	VGA_CODE[3:0]	IF vga manual gain control 0000: -12.0 dB 1111: +40.5 dB; -3.5dB/step
R13 0x0D	R/W	[7:4]	LNA_VTHH[4:0]	LNA agc power detector voltage threshold high setting 1111: 1.94 V 0000: 0.34 V, ~0.1 V/step
	R/W	[3:0]	LNA_VTHL[3:0]	LNA agc power detector voltage threshold low setting 1111: 1.94 V 0000: 0.34 V, ~0.1 V/step
R14 0x0E	R/W	[7:4]	MIX_VTH_H[4:0]	MIXER agc power detector voltage threshold high setting 1111: 1.94 V 0000: 0.34 V, ~0.1 V/step
	R/W	[3:0]	MIX_VTH_L[3:0]	MIXER agc power detector voltage threshold low setting 1111: 1.94 V 0000: 0.34 V, ~0.1 V/step

Reg	R/W	Bitmap	Symbol	Description
R15 0x0F	R/W	[4]	CLK_OUT_ENB	Clock out pin control 0: clk output on 1: off
	R/W	[1]	CLK_AGC_ENB	AGC clk control 0: internal agc clock on 1: off
R16 0x10	R/W	[7:5]	SEL_DIV[3:0]	PLL to Mixer divider number control 000: mixer in = vco out /2 001:mixer in = vco out / 4 010: mixer in = vco out / 8 011:mixer in = vco out
	R/W	[4]	REFDIV	PLL Reference frequency Divider 0 -> fref=xtal_freq 1 -> fref=xta_freql / 2 (for Xtal >24MHz)
	R/W	[1:0]	CAPX[1:0]	Internal xtal cap setting 00->no cap ; 01->10pF 10->20pF ; 11->30pF
R17 0x11	R/W	[7:6]	PW_LDO_A[1:0]	PLL analog low drop out regulator switch 00: off 01: 2.1V 10: 2.0V 11: 1.9V
R20 0x14	R/W	[7:6]	SI2C[1:0]	PLL integer divider number input Si2c Nint=4*Ni2c+Si2c+13 PLL divider number Ndiv = (Nint + Nfra)*2
	R/W	[5:0]	NI2C[5:0]	PLL integer divider number input Ni2c
R21 0x15	R/W	[7:0]	SDM_IN[7:0]	PLL fractional divider number input SDM[16:1] Nfra=SDM_IN[16]*2^-1+SDM_IN[15]*2^-2+…+SDM_IN[2] *2^-15+SDM_IN[1]*2^-16
R22 0x16	R/W	[7:0]	SDM_IN[7:0]	

Reg	R/W	Bitmap	Symbol	Description
R23 0x17	R/W	[7:6]	PW_LDO_D[1:0]	PLL digital low drop out regulator supply current switch 00: 1.8V,8mA 01: 1.8V,4mA 10: 2.0V,8mA 11: OFF
	R/W	[3]	OPEN_D[3]	Open drain 0: High-Z 1: Low-Z
R25 0x19	R/W	[7]	PWD_RFFILT	RF Filter power 0: off 1:on
	R/W	[4]	SW_AGC	Switch agc_pin 0:agc=agc_in 1:agc=agc_in2
R26 0x1A	R/W	[7:6]	RFMUX[1:0]	Tracking Filter switch 00: TF on 01: Bypass
	R/W	[3:2]	PLL_AUTO_CLK[1:0]	PLL auto tune clock rate 00: 128 kHz 01: 32 kHz 10: 8 kHz
	R/W	[1:0]	RFFILT[1:0]	RF FILTER band selection 00: highest band 01:med band 10:low band
R27 0x1B	R/W	[7:4]	TF_NCH[1:0]	0000 highest corner for LPNF; 1111 lowerst corner for LPNF
	R/W	[3:0]	TF_LP[3:0]	0000 highest corner for LPF; 1111 lowerst corner for LPF
R28 0x1C	R/W	[7:4]	PDET3_GAIN[1:0]	Power detector 3 TOP(take off point) control 0: Highest : 15: Lowest

Reg	R/W	Bitmap	Symbol	Description
R29 0x1D	R/W	[5:3]	PDET1_GAIN[2:0]	Power detector 1 TOP(take off point) control 0: Highest : 15: Lowest
	R/W	[2:0]	PDET2_GAIN[2:0]	Power detector 2 TOP(take off point) control 0: Lowest : 7: Highest
R30 0x1E	R/W	[5:0]	PDET_CLK[5:0]	Power detector timing control 111111: max : 000000: min
	R/W	[6]	FILTER_EXT	Filter extension under weak signal 0: Disable 1: Enable